UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,291	04/13/2004	Hidehiko Suzuki	08211/0200655-US0/P05800	4557

38845 7590 11/30/2005

DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/823,291	**Applicant(s)** SUZUKI, HIDEHIKO	
	Examiner Thomas J. Hiltunen	**Art Unit** 2816	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 14 November 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☒ Newly proposed or amended claim(s) *21* would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: *21 and 23*.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-10,12 and 22-24*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See attached sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

Response to Arguments

With respect to claims 1-10, examiner finds applicant's arguments unpersuasive. Applicant's arguments do not concern operation at the certain point, which is the threshold of the logic circuit. Applicant states that in the specification that threshold of the logic circuit is at VDD/2. Thus Kong et al. still reads over the claim language when the IN voltage is at VDD/2. It can be seen that when IN is VDD/2, N1 will have a voltage of VDD/2, which will input to capacitor Cp. Capacitor Cp is charged to VDD, thus the voltage present at the source of M4 will be

VDD/2 (voltage at N1) – VDD (voltage charged in Cp), which equals -VDD/2. At this point, it can be seen that M4 will be on much harder than M3. This means when IN is equal to VDD/2, approximately - VDD/2 will be output by M4 to PMOS transistor M1 (because M4 is on harder (VGS > VSG) than M3). Therefore M1's source to gate voltage will be VDD - - VDD/2, which equals 3VDD/2 and is greater than VDD/2 ("mid-supply voltage"). At the same time (when IN equals VDD/2), M2 will output a similar value to the complementary configuration of circuit.

Further, it is noted that the drawing for Fig. 2 is incorrectly shows VOUT maintaining a constant voltage level throughout tdelay, and then, almost instantly, reaches 0 volts at the end of t_{dealy}. However, it would have been well understood by one of ordinary skill in the art that VOUT decreases (in a linear fashion) throughout t_{delay} until VOUT reaches 0 volts.

With respect to claim 3 and 12, examiner finds applicant's arguments unpersuasive. Again, a capacitor can be seen to provide a resistance, for the reasons stated previously. Applicant's arguments relate to a "resistor" not a "resistor circuit".

With respect to claim 22, examiner finds applicant's arguments unpersuasive. It can be seen that the effective voltage is 3VDD/2 as explained above in the response to the arguments of claims 1-10.

With respect to claim 24, examiner finds applicant's arguments unpersuasive. The word coupled is understood to mean to have a connection, which can include a physical connection through intermediary elements. If the applicant whishes read over the citied art, a direct connection or an "electrical coupling regardless of logic state" between the PMOS transistor and capacitor should be claimed.

Allowable Subject Matter

With respect to claim 21, examiner agrees with applicant. There it is now clear that Vdd is chosen to be a "high supply voltage", and thus cannot be read as an arbitrary value within the combination of Kong et al. and Sanwo et al.. The pull-up resistor would be part of a voltage offset circuit. However, the offset circuit does not output a value approximately equal to VDD +I1*R1, where VDD + I1*R1 is equal to the difference between a high and low voltage. Therefore claim 21 is deemed allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571) 272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner

TH
November 23, 2005